WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor, comprising steps of:

(a) providing an insulating substrate;

(b) sequentially forming a source/drain layer, a primary gate insulating layer, and a first conducting layer on said insulating substrate;

(c) etching said first conducting layer to form a primary gate;

(d) sequentially forming a secondary gate insulating layer and a second conducting layer on said primary gate; and

(e) etching said second conducting layer to form a first secondary gate and a second secondary gate.

2. The method according to claim 1, wherein said insulating substrate is a glass.

3. The method according to claim 1, wherein said source/drain layer is a high-doping semiconductor layer.

4. The method according to claim 3, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

5. The method according to claim 1, wherein said source/drain layer comprises a drain, a channel and a source.

6. The method according to claim 5, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said secondary insulating layer, a length of said first secondary gate and a length of said second secondary gate.

7. The method according to claim 1, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

8. The method according to claim 1, wherein said first conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum

molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

9. The method according to claim 1, wherein said step (c) is executed by means of a reactive ion etching.

10. The method according to claim 1, wherein said secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

11. The method according to claim 1, wherein said second conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

12. The method according to claim 1, wherein said step (e) is executed by means of a reactive ion etching.

13. A structure of a thin film transistor comprising:

an insulating substrate;

a source/drain layer disposed on said insulating substrate;

a primary insulating layer disposed on said source/drain layer;

a primary gate disposed on said primary insulating layer;

a secondary insulating layer disposed on said primary insulating layer; and

a secondary gate disposed on said secondary insulating layer and insulated from said primary gate via said secondary insulating layer.

14. The structure according to claim 13, wherein said secondary insulating layer further comprises a first secondary insulating layer and a second secondary insulating layer.

15. The structure according to claim 14, wherein said secondary gate further comprises a first secondary gate and a second secondary gate disposed on said first secondary insulating layer and said second secondary insulating layer respectively.

16. The structure according to claim 13, wherein said insulating substrate is a glass.

17. The structure according to claim 13, wherein said source/drain layer is a high-doping semiconductor layer.

18. The structure according to claim 17, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

19. The structure according to claim 13, wherein said source/drain layer comprises a drain, a channel and a source.

20. The structure according to claim 19, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said secondary insulating layer, and a length of said secondary gate.

21. The structure according to claim 13, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

22. The structure according to claim 13, wherein said first conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

23. The structure according to claim 13, wherein said primary gate is formed by means of a reactive ion etching.

24. The structure according to claim 13, wherein said secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

25. The structure according to claim 13, wherein said second conducting layer is one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

26. The structure according to claim 13, wherein said secondary gate is formed by means of a reactive ion etching.

27. A structure of a thin film transistor comprising:

an insulating substrate;

a source/drain layer disposed on said insulating substrate;

a primary insulating layer disposed on said source/drain layer;

a primary gate disposed on said primary insulating layer;

at least a secondary insulating layer disposed on said primary insulating layer; and

at least a secondary gate disposed on said at least a secondary insulating layer and insulated from said primary gate via said at least a secondary insulating layer.

28. The structure according to claim 27, wherein said insulating substrate is a glass.

29. The structure according to claim 27, wherein said source/drain layer is a high-doping semiconductor layer.

30. The structure according to claim 29, wherein said high-doping semiconductor layer is high-doping polycrystalline silicon.

31.The structure according to claim 27, wherein said source/drain layer comprises a drain, a channel and a source.

32.The structure according to claim 31, wherein said channel has a length equal to a sum of a length of said primary gate, a width of said at least secondary insulating layer, and a length of said at least a secondary gate.

33.The structure according to claim 27, wherein said primary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.

34.The structure according to claim 29, wherein said at least a secondary gate insulating layer is one selected from a silicon nitride (SiN_x), a silicon oxide (SiN_x), a silicon oxide nitride (SiO_xN_y), a tantalum oxide (TaO_x), an aluminum oxide (AlO_x) and a mixture thereof.